SADC developments for PANDA
Initial SADC developments

<table>
<thead>
<tr>
<th>ADC Model</th>
<th>AVM16 / AVX16</th>
<th>FQDC-240</th>
<th>FQDC-160</th>
<th>SQDC-80</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of channels</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>160/250 MHz</td>
<td>240 MHz</td>
<td>160 MHz</td>
<td>80 MHz</td>
</tr>
<tr>
<td>Input coupling</td>
<td>DC /AC (5 μs)</td>
<td>AC (5 μs)</td>
<td>AC (5 μs)</td>
<td>DC</td>
</tr>
<tr>
<td>Resolution</td>
<td>12-bit</td>
<td>±11-bit</td>
<td>±11-bit</td>
<td>12-bit</td>
</tr>
<tr>
<td>Baseline</td>
<td>DAC controlled</td>
<td>0 V</td>
<td>0 V</td>
<td>DAC controlled</td>
</tr>
<tr>
<td>Data retention</td>
<td>6.4 μs</td>
<td>6.4 μs</td>
<td>6.4 μs</td>
<td>12.8 μs</td>
</tr>
<tr>
<td>Input filter</td>
<td>Passive CR</td>
<td>Passive CR</td>
<td>Passive CR</td>
<td>Active filter</td>
</tr>
<tr>
<td>Interface</td>
<td>VME-64x /VXS</td>
<td>LVD-BUS(1)</td>
<td>LVD-BUS(1)</td>
<td>LVD-BUS(1)</td>
</tr>
</tbody>
</table>

Feature extraction:
- Signal search within window
- Partial integrals
- Arrival times
- Maxima, minima
- Baseline and noise

### ADC Model: PANDA_16

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td><strong>No. of channels</strong></td>
<td>16</td>
</tr>
<tr>
<td><strong>Sampling rate</strong></td>
<td>125 MSPS</td>
</tr>
<tr>
<td><strong>Input coupling</strong></td>
<td>DC/AC (5 μs)</td>
</tr>
<tr>
<td><strong>Resolution (amplitude)</strong></td>
<td>14-bit</td>
</tr>
<tr>
<td><strong>Baseline</strong></td>
<td>DAC controlled</td>
</tr>
<tr>
<td><strong>Input range</strong></td>
<td>±1.0V or -2V..0V</td>
</tr>
<tr>
<td><strong>Noise</strong></td>
<td>1.8 bit σ, 200μV</td>
</tr>
<tr>
<td><strong>Data retention</strong></td>
<td>6.4 μs</td>
</tr>
<tr>
<td><strong>Input filter</strong></td>
<td>Passive CR-filter</td>
</tr>
<tr>
<td><strong>Interface</strong></td>
<td>Optical, SFP, LC-type, 2 Gbit/s</td>
</tr>
<tr>
<td><strong>Feature extraction:</strong></td>
<td>Signal search within window</td>
</tr>
<tr>
<td></td>
<td>Partial integrals</td>
</tr>
<tr>
<td></td>
<td>Arrival times</td>
</tr>
<tr>
<td></td>
<td>Maxima, minima</td>
</tr>
<tr>
<td></td>
<td>Baseline and noise</td>
</tr>
</tbody>
</table>
# SADC development for PANDA EMC

<table>
<thead>
<tr>
<th>ADC Model</th>
<th>ADC_32DR</th>
<th>ADC_64V</th>
<th>ADC_64K</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of channels</td>
<td>32 (64)</td>
<td>64</td>
<td>64</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>80-125 MSPS</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>Input coupling</td>
<td>DC, positive, negative, diff</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>Resolution (ampl)</td>
<td>14-bit dual range</td>
<td>14-bit</td>
<td></td>
</tr>
<tr>
<td>Input Connector</td>
<td>uFL</td>
<td>Samtec</td>
<td></td>
</tr>
<tr>
<td>Baseline</td>
<td>0V</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>Input range (dual)</td>
<td>±1.0V, ±100 mV</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>Noise</td>
<td>?</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>Data retention</td>
<td>?</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>Input filter</td>
<td>Active-filter/Amplifier</td>
<td>CR-passive</td>
<td>Active filter/Amplifier</td>
</tr>
<tr>
<td>Interface</td>
<td>Optical, SFP, LC-type, 2 Gbit/s</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>Feature extraction:</td>
<td>Signal search within window</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Partial integrals</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Arrival times</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Maxima, minima</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Baseline and noise</td>
<td>64</td>
<td></td>
</tr>
</tbody>
</table>
ADC for EMC-Endcap
- Ready prototype
4 dual-range channels (8 ADC 14-bit channels)
ADC for EMC-Endcap
- Ready prototype
**Power supply**
High efficiency (DC/DC), ferrite-less (Air-Core)

**Amplifier**
Fully differential, BW > 100 MHz, SR > 100 V/us, Pd < 50 mW/ch, Active filter

**ADC**
- G=1
- G=16
- 16-ch dual range block
- 8-ch ADC
- 14-bit
- 80 Ms/s

**FPGA**
- Virtex-6
- Optical Interface
- Clocking, Configuration
- Common, dual accessible

**SerDes**
Radiation immune, SODA-compliant, dual

**Design Idea**
- ADC for EMC-Endcap
- 32 inputs
- Positive, Negative or Differential
- +/- 1V FS
- +/- 60 mV FS
- 16-ch dual range block
- Shaper/Amplifier
- G=1
- G=16
- 8-ch ADC
- 14-bit
- 80 Ms/s
- FPGA
- Virtex-6

**Clocking, Configuration**
- Common, dual accessible

**FPGA**
- Radiation immune
- (RT-Flash or Tripple Modular Redundancy)
or partially reconfigurable with watchdog, 32/64 channels per board

**ADC**
- EOB > 14-bit
- Sampling rate ~ 80Ms/s
- Pd < 100 mW/ch
- 32 (64) ch. per board

**Amplifier**
- Fully differential, BW > 100 MHz
- SR > 100 V/us
- Pd < 50 mW/ch
- Active filter
ADC for EMC-Endcap
– identifying components

KVI – shaper / active filter

(by Franz Schreuder)
ADC for EMC-Endcap
- 60 mV pulse - bipolar

G = 1

G = 16
ADC for EMC-Endcap
-1V pulse - bipolar

G = 1
G = 16

ADC for EMC-Endcap
- Cross-talk

Adjacent channel, \( G = 16 \)

1V input pulse, \( G = 1 \)

Adjacent channel, \( G = 16 \)
ADC for EMC-Endcap
- Noise tracks

G = 16

G = 1

ADC for EMC-Endcap

- Noise track

G = 16

G = 1
ADC for EMC-Endcap

Noise – amplitude spectrum

ADC noise

- G = 1
- G = 16

Occurrence

ADC value

Improving resolution using dual-range by a 16x follower

Courtesy Malte Albrecht
ADC for EMC-Endcap
- Encapsulation and Cooling

Courtesy KVI
ADC for EMC-Endcap
- Encapsulation and Cooling

Courtesy KVI
ADC for EMC-Endcap
- Preparation for the PbWO$_4$/VPTT tests at Max Lab

PbWO$_4$ + VPTT

ADC32DR

ATLB (VME Optical Data Concentrator)

VME
ADC for EMC-Endcap
- Development - Time plan

**V1.1 – June 2013**
* Design clean-up
* Block connectors – Samtec ERF8-049-XX-X-D-RA
* 64 – channels with individual gain, no filter

**V1.2 – August 2013**
* Block connectors
* Low power op-amp ADA4940-2
* 32-ch. with gain $G = 0.5$, filtered
* 32-ch. with gain $G = 5.0$, filtered

**V2.0 – October 2013**
* Kintex-7
### ADC for EMC-Endcap

**Input**

**Connector**

- **ADC32DR (V1.0)**
  - Input Connector: 64 x uFL
  - Input Amp Config:
    - 32 ch. Dual Range
    - Filtered, gain x1 followed by 16x LTC6403
    - Full SODA: No
    - FPGA: Virtex-6
    - Status: First prototype, Manufactured and tested Operational

- **ADC64V (V1.1)**
  - Input Connector: Samtec
  - Input Amp Config:
    - 64 ch. independent,
    - No filter, Gain 1.0
    - LTC6403
    - Full SODA: Yes
    - FPGA: Virtex-6
    - Comment: Bug fixed ADC32DR with input modification
    - Status: Design ready.

- **ADC64VA (V1.2)**
  - Input Connector: Samtec
  - Input Amp Config:
    - 64 ch. Independent
    - 32 Filtered, Gain 0.5
    - 32 Filtered, Gain 5.0
    - ADA4940-2
    - Full SODA: Yes
    - FPGA: Virtex-6
    - Comment: Bug fixed ADC32DR with input modification
    - Status: Design ready. Purchase interest expressed by KVI

- **ADC64K (V2.0)**
  - Input Connector: Samtec
  - Input Amp Config:
    - 64 ch. Independent
    - 32 Filtered, Gain 0.5
    - 32 Filtered, Gain 5.0
    - ADA4940-2
    - Full SODA: Yes
    - FPGA: Kintex-7
    - Comment: Bug fixed ADC32DR with input modification
    - Status: Design in progress. Expected ready by 30.09
ADC for EMC-Endcap - Connections

**Board Connector**

![Board Connector Image]

**Backplane solution**

![Backplane Solution Image]

**Direct cable connection solution**

![Direct Connection Image]

- ERF8-049-XX-X-D-RA
- ERDP
  - 0,80 mm Edge Rate™
  - High Speed Twinax Cable Assembly
- ERCD
  - 0,80 mm Edge Rate™
  - High Speed Coax Cable Assembly

Pawel Marciniewski, PANDA Collab. Meeting, Bochum, 10.09.2013
### ADC for EMC-Endcap

- **Power requirements**

#### Analog (LDO filtered)

<table>
<thead>
<tr>
<th>Voltage</th>
<th>V1.0</th>
<th>V2.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>+2.2V (1.8V) – 3.2A (ADC)</td>
<td>7.0 W</td>
<td>7.0 W</td>
</tr>
<tr>
<td>+2.9V (2.5V) – 1A (AMP)</td>
<td>2.9 W</td>
<td>0.4 W</td>
</tr>
</tbody>
</table>

#### Digital

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>+1.0V – 6A (FPGA)</td>
<td>6.0W</td>
</tr>
<tr>
<td>+1.2V – 1.2A (FPGA)</td>
<td>1.5W</td>
</tr>
<tr>
<td>+1.8V - 0.8A (ADC)</td>
<td>1.5W</td>
</tr>
<tr>
<td>+2.5V – 3.0A (FPGA)</td>
<td>7.5W</td>
</tr>
<tr>
<td>+3.3V – 0.4A (PLL), 0.5A(SFP)</td>
<td>1.3W</td>
</tr>
</tbody>
</table>

---

**TOTAL NETTO POWER**

<table>
<thead>
<tr>
<th></th>
<th>V1.0</th>
<th>V2.0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>28 W</td>
<td>20W</td>
</tr>
</tbody>
</table>

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Thank You!

Special thanks to Frans Schreuder, Peter Schakel